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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,681	01/28/2002	Ming-Nan Yen	JCLA7301	4020

23900 7590 07/25/2005

J C PATENTS, INC.
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EXAMINER	
GHEBRETINSAE, TEMESGHEN	
ART UNIT	**PAPER NUMBER**
2637	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/058,681	YEN ET AL.	
	Examiner	Art Unit	
	Temesghen Ghebretinsae	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *06 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8,9 and 11-14* is/are rejected.

7)☒ Claim(s) *3,7,10 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It would be of great assistance to the Office if all incoming papers pertaining to a filed application carried the following items:

1. Application number (checked for accuracy, including series code and serial no.).
2. Group art unit number (copied from most recent Office communication).
3. Filing date.
4. Name of the examiner who prepared the most recent Office action.
5. Title of invention.
6. Confirmation number (See MPEP § 503).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1,5,9 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al (6,392,496).

Lee discloses a digital phase locked loop (fig.1) comprising: a phase detector (1) for comparing a feedback signal and a reference signal; a digital to analog converter (4) for converting the digital phase outputted from the phase comparator; a voltage control oscillator; (5) **and an adjustable divider (6)** for feeding back (a feedback signal with a feedback frequency) and dividing down the output from the VCO. (See col.1, lines 17-37)

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1,5,6,9,11,13 are rejected under 35 U.S.C. 102(b) as being anticipated by Wereker et al (5,856,762).

Wereker discloses a digital phase locked loop comprising: a phase detector for comparing a feedback signal and a reference signal (51); a digital to analog converter for converting the digital phase to analog phase signal (53); a voltage control oscillator (4) and **a post divider (13)** for feeding back (a feedback signal with a feedback frequency) and dividing down the output from the VCO (13) as claimed in claim1. An up-down converter (52) as claimed in claim 6. The post adjusting value for the post divider is adjustable (N) as claimed in claim 9. The feedback signal has a preset value as claimed in claim 11. The post adjusting value is set according to the required output frequency as claimed in claim 13. (See fig.1 and col.3, line 40 to col.4, line 6.

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1,5,6,9,11,13 are rejected under 35 U.S.C. 102(a) as being anticipated by Walter T. Bax et al (A GMSK modulator using a delta sigma frequency discriminator based synthesizer IEEE Journal of solid state circuits vol. 36, No. 8 August 2001).

Bax et al discloses a digital phase locked loop comprising: a phase-frequency detector for comparing a feedback signal and a reference signal; a digital to analog converter; a voltage control oscillator; a post divider for feeding back and dividing down the output from the VCO; and an up-down converter. (See fig.3

and fig.11). The post adjusting value for post divider is adjustable (The feedback signal has a preset value (see page 1220 second col.). The post adjusting value is set according to the required output frequency. (See pages 1218-1223).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2,4,6,8,11,12,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Berry et al (6,366,174).

Lee discloses the claimed subject matter as described above. Lee differs from the present claimed invention in that he is silent about pre-divider as claimed in claim 2 and 12; out put divider as claimed in claim 4 and 14;and up-down converter as claimed in claim 6. However, Berry discloses a phase locked loop apparatus comprising: an adjustable pre-divider for dividing down the input signal (20); and adjustable output divider (44); and up-down converter (30). Thus it would have been obvious to one of ordinary skill in the art at the time the invention to modify Lee's PLL circuit to show the pre-diver, output divider and up-down counter. One would be motivated to do so because having a PLL circuit with optional frequency multiply or frequency divide circuits can improve the latch

time. (See Berry col.2, lines 1-15. and fig.1) As for the built-in self tester, such is well know in the art (see specification page 8, lines 21-22.)

8. Claims 2,4,12,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Werker in view of Berry

Werker disclose the subject matters claimed in claims 1,5,6,9,11,13 as described above. Werker differs from the present invention in that he is silent about pre-divider as claimed in claim 2 and 12; out put divider as claimed in claim 4 and 14. However, such are well know in the PLL circuit and would have been obvious to have a PLL circuit with optional frequency multiply or frequency divide circuits so that the latch (lock) time can be improved. (See Berry col. 2, lines 1-15 and fig.1) As for the particular limitation of claim 15, Berry is silent about the value of the digital signal (N). However, such is well known and does not show any new or unexpected result.

9. Claims 2, 4,12,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bax in view of Berry

Bax discloses all the subject matter claimed in claims 1,5,6,9,11,13 see above. Bax differs from the claimed invention in that he is silent about pre-divider as claimed in claim 2 and 12; out put divider as claimed in claim 4 and 14. However, such are well know in the PLL circuit and would have been obvious to have a PLL circuit with optional frequency multiply or frequency divide circuits so that the latch (lock) time can be improved. (See Berry col. 2, lines 1-15 and fig.1)

Allowable Subject Matter

10. Claim 3,7,10,15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

11. Applicant's arguments filed 5/6/05 have been fully considered but they are not persuasive. Applicant argues that Lee (6,392,496) or Wereker (5,856,762) or Walter T. Bax do not disclose a feedback signal with a feedback frequency and a post-divider. However, examiner disagree with the applicant's conclusion because all of them Lee (6,392,496) or Wereker (5,856,762) or Walter T. Bax disclose a feedback signal with a feedback frequency and a post-divider. See post-diver (6) in Lee; post divider (13) in Wereker and Multi modulus divider in Bax, generating a feedback signal with a feedback frequency.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Temesghen Ghebretinsae whose telephone number is 571-272-3017. The examiner can normally be reached on Monday-Friday from 8 to 5. The examiner can also be reached on alternate

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel, can be reached on 572-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Temesghen Ghebretinsae
Primary Examiner
Art Unit 2637

T.G.

7/19/05

7/19/05
TEMESGHEN GHEBRETINSAE
PRIMARY EXAMINER